Customer No.: 31561
Application No.: 10/710,818
Docket NO.: 14217-US-PA-X

REMARKS

Present Status of the Application

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the AAPA of this application in combination with Shokouhi et al. (US patent 6,249,458).

Discussion of Office Action Rejections

In response to the rejections to claims 1-10 under 35 U.S.C. 103(a) as being unpatentable over the AAPA of this application in combination with Shokouhi et al. (US patent 6,249,458), Applicants hereby submit that the present invention, as set forth in claim 1 is neither taught, suggested, nor disclosed by the AAPA, Shokouhi et al. (US patent 6,249,458, or any other cited references, taken alone or in combination.

With respect to claim 1, as originally filed, recites:

An electrostatic discharge (ESD) protection device, comprising:
an ESD protection circuit, comprising:
at least a diode connected in series between a first voltage and a pad; and
at least an ESD component connected in series between a second voltage and a pad, wherein ***each of the at least an ESD component comprises a deep N-well region formed in a P-type substrate, a triple P-well formed in the deep N-well region, and a highly doped N-type (N+) region and a highly doped P-type (P+) region formed in the triple P-well region.***

The Office Action points out AAPA teaches forming the highly doped N-type region and highly doped P-type region in N-well region that is formed in a P-type substrate but fails to teach

forming the highly doped N-type region and highly doped P-type region in a triple P-well located in a deep N-well region that is formed in a P-type substrate. Shokouhi et al. teach forming a device in a triple P-well located in a deep N-well region that is formed in a P-type substrate to limit or prevent leakage current. It would have been obvious to one skilled in the art of making semiconductor devices to incorporate the above teaching of Shokouhi et al. into the structure of AAPA to prevent leakage current.

However, in ***claim 1*** of the present invention, the highly doped N-type region and highly doped P-type region formed in a triple P-well located in a deep N-well region that is formed in a P-type substrate is ***for reducing the parasitic capacitance and substrate noise of the ESD device.*** The objective of the claimed invention is not limiting or preventing leakage current.

To one of ordinary skill in the art, with mere a teaching given by Shokouhi of preventing leakage current, Shokouhi '458 teaches, if any, away from combining "forming a device in a triple P-well located in a deep N-well region that is formed in a P-type substrate" with the AAPA. Therefore, Applicants submit that the present invention as set forth in claim 1 should not be considered as obvious over the AAPA in view of Shokouhi '458.

The Examiner alleged that the fact that the Applicants have a different reason or advantage resulting from doing what the relied prior art suggested doing is not indicative or demonstrative of unobviousness. However, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re* Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

Further, the point of argument is not the difference between the advantages of respectively the present invention and the prior art. The point is there is no teaching or suggestion to make the claimed combination and the reasonable expectation of success found in the cited references. Without such teaching or suggestion, the combination between the cited references can not render the present invention obvious. MPEP §2143.

Furthermore, the device of Fig. 7 disclosed by Shokouhi et al. is ***a triple P-well resistor including two P-doped regions 731, 733*** in the triple P-well 730 formed in the deep N-well 720 that is formed in a P-substrate 710, and the deep N-well 720 is biased by a system voltage (Vcc) and the P-substrate 710 is grounded, thereby reverse biasing the central P-well region to limit leakage current from the P-well region. However, the device in claim 1 is ***an ESD component including a highly doped N-type region and a highly doped P-type region*** formed in a triple P-well located in a deep N-well region that is formed in a P-type substrate. Apparently, the function and the structure of the device disclosed by Shokouhi et al. are much different from the ESD component of claim 1 in structure. Thus, even combined with each other, the AAPA and Shokouhi '458 do not teach or suggest all of the limitations, as set forth in claim 1. MPEP §2143.03

For at least the foregoing reasons, Applicant respectfully submits that independent claim 1 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-10 patently define over the prior art as a matter of law.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-10 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

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